

Fig. 1

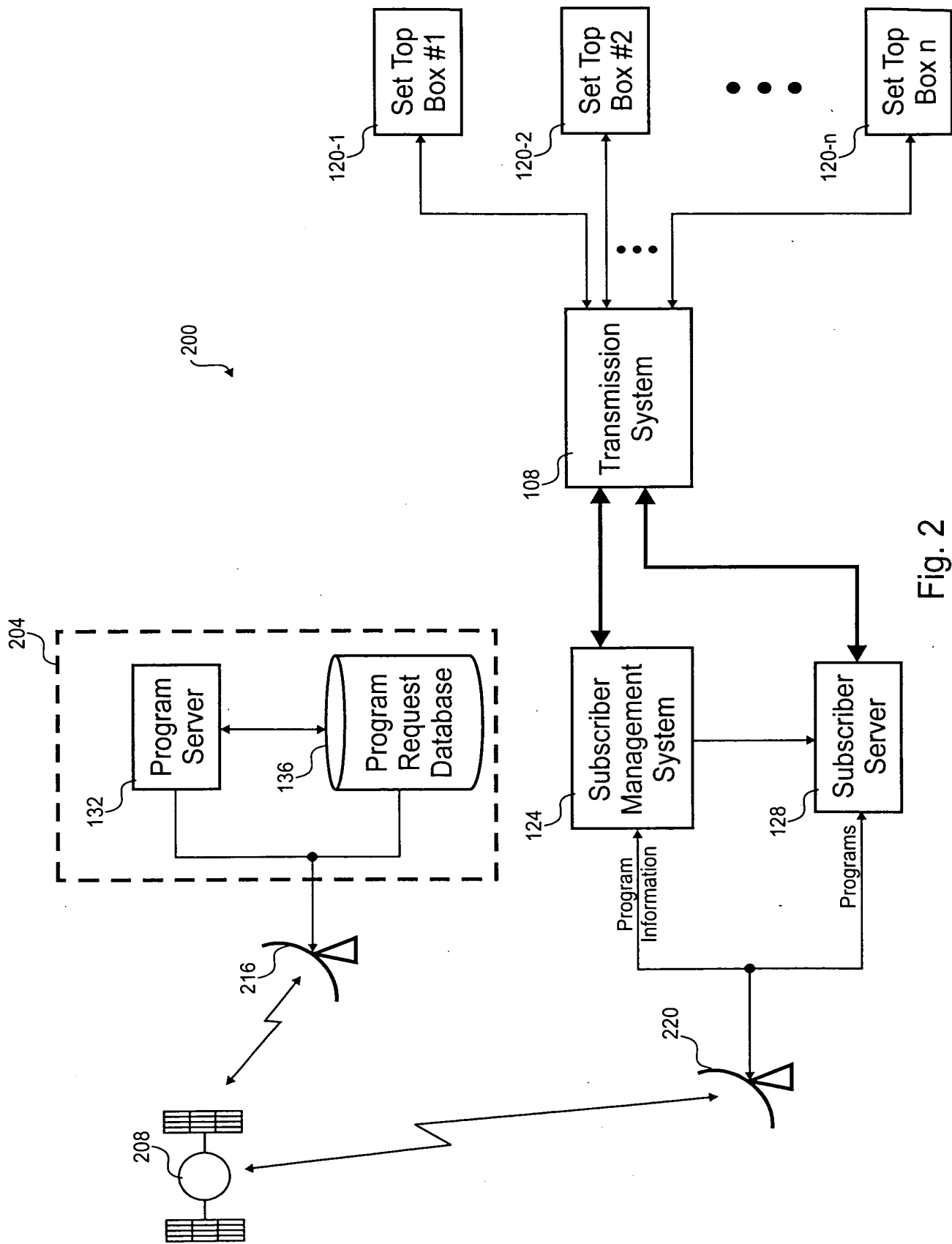


Fig. 2

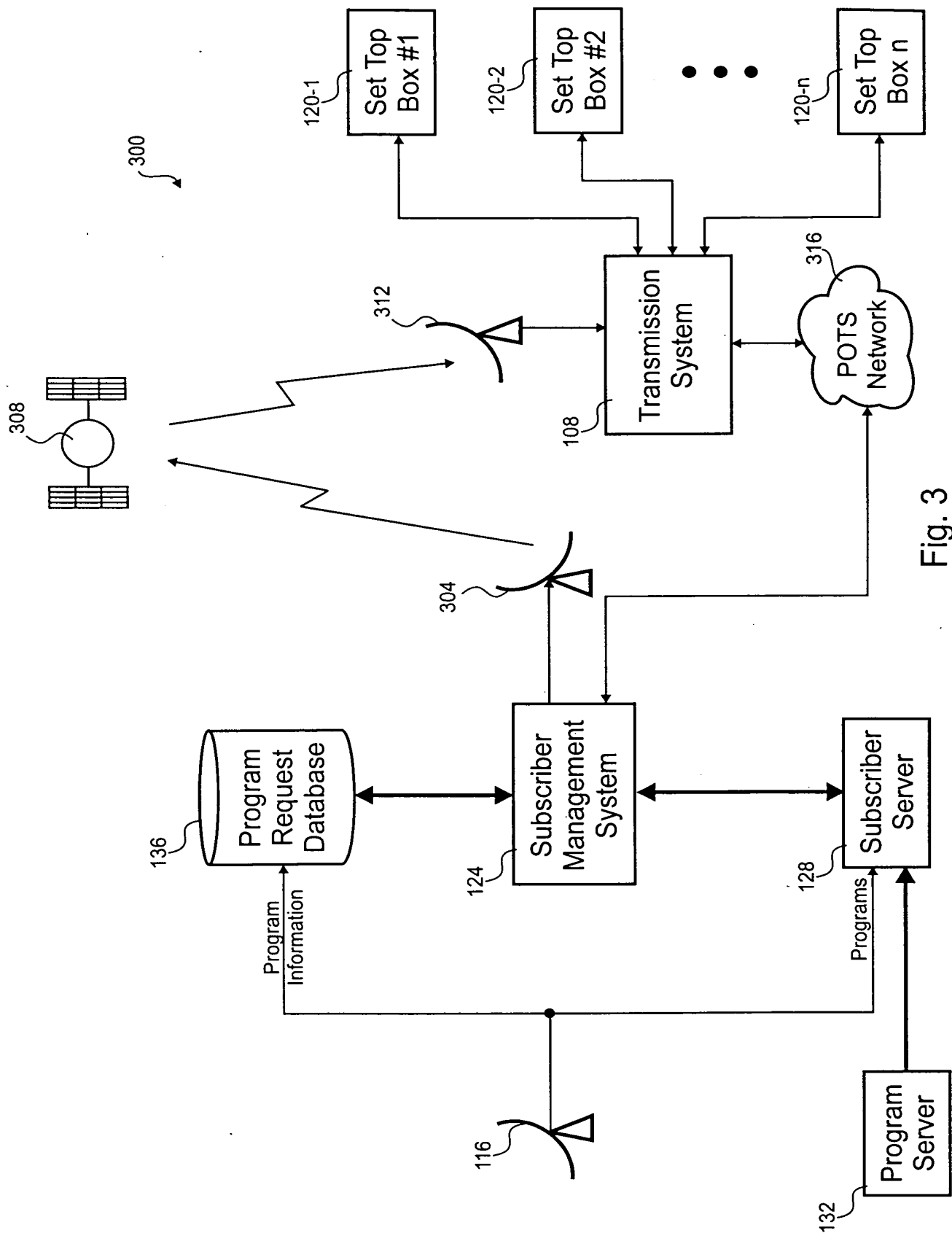


Fig. 3

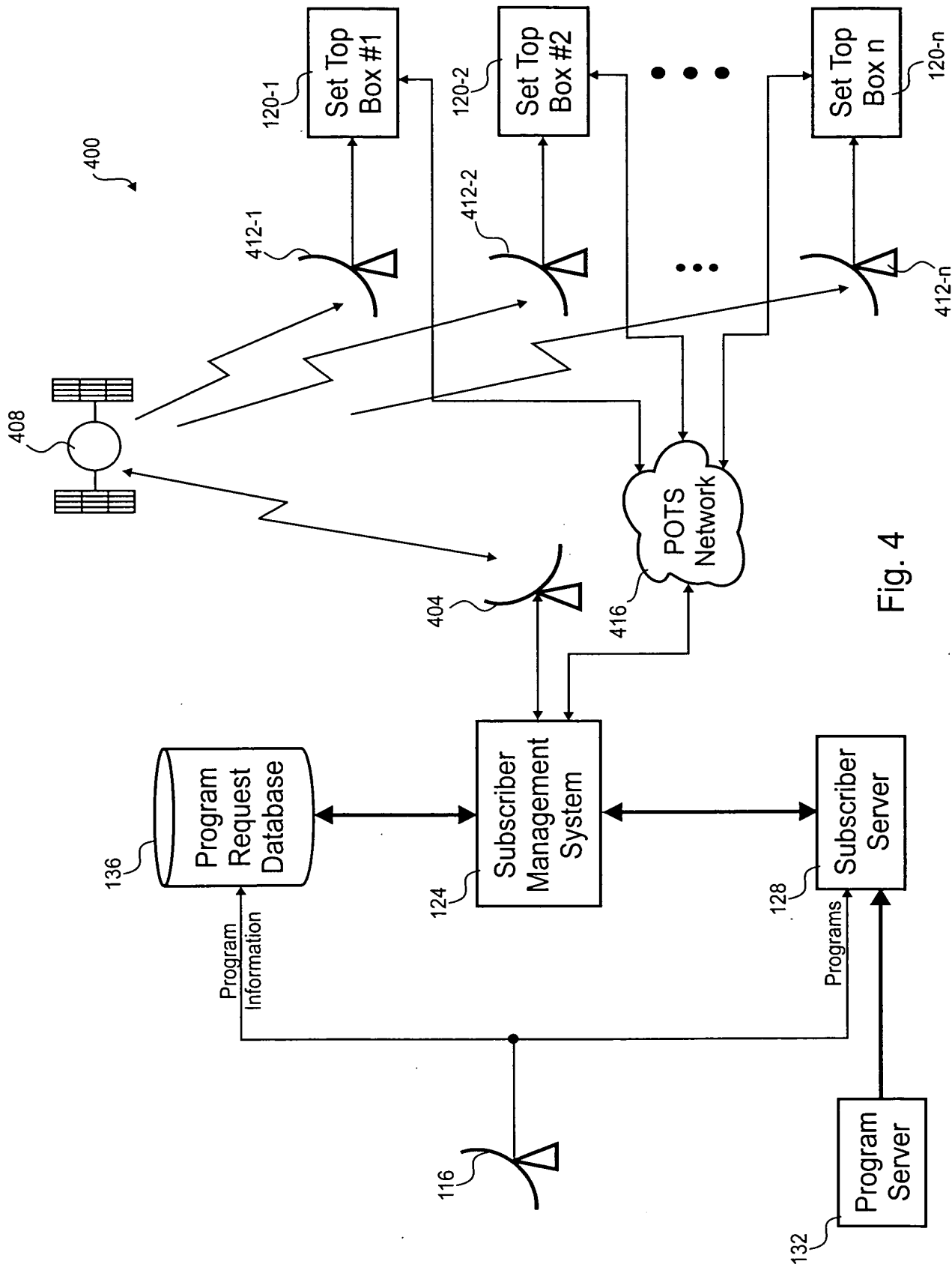


Fig. 4

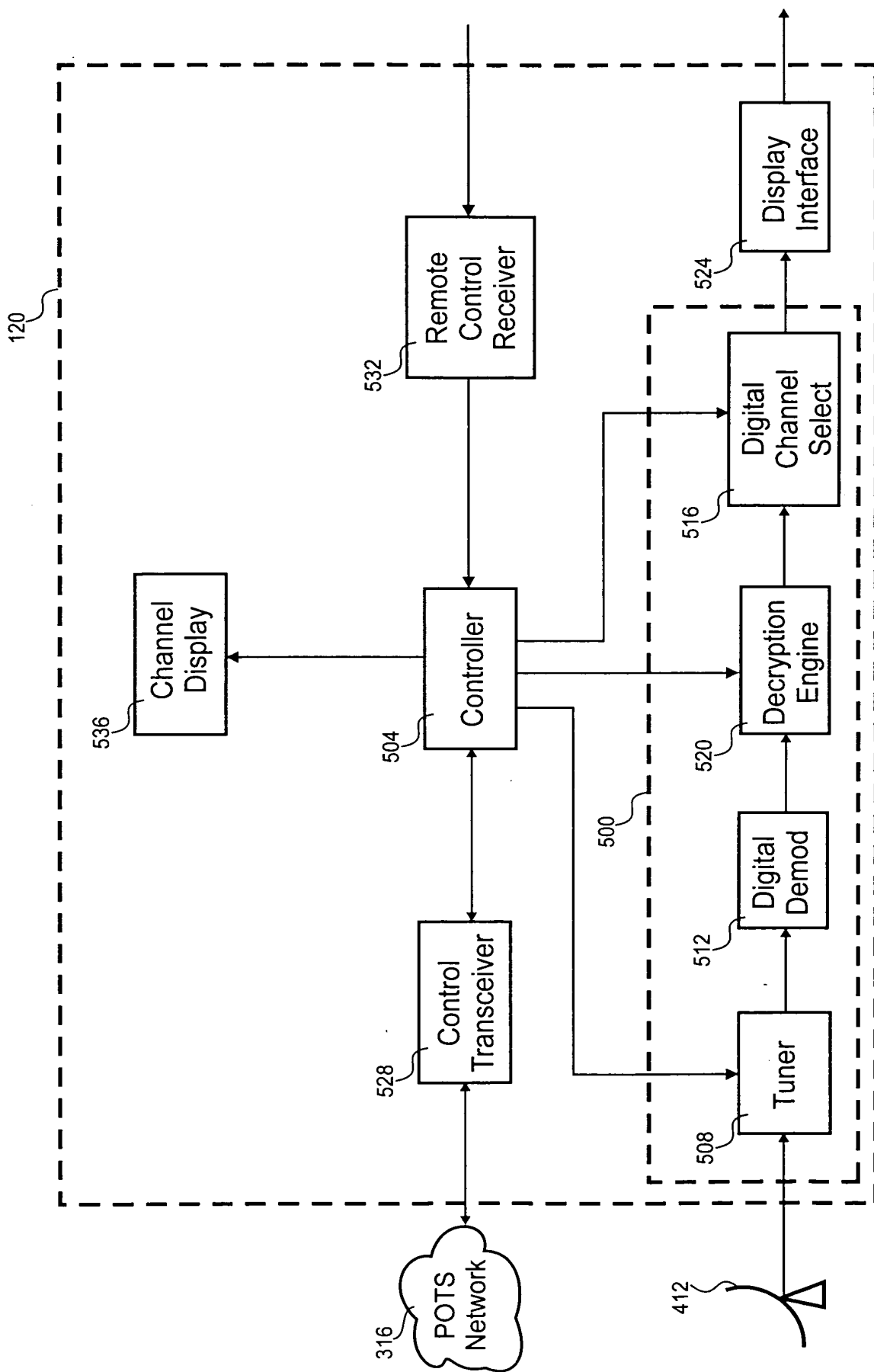


Fig. 5

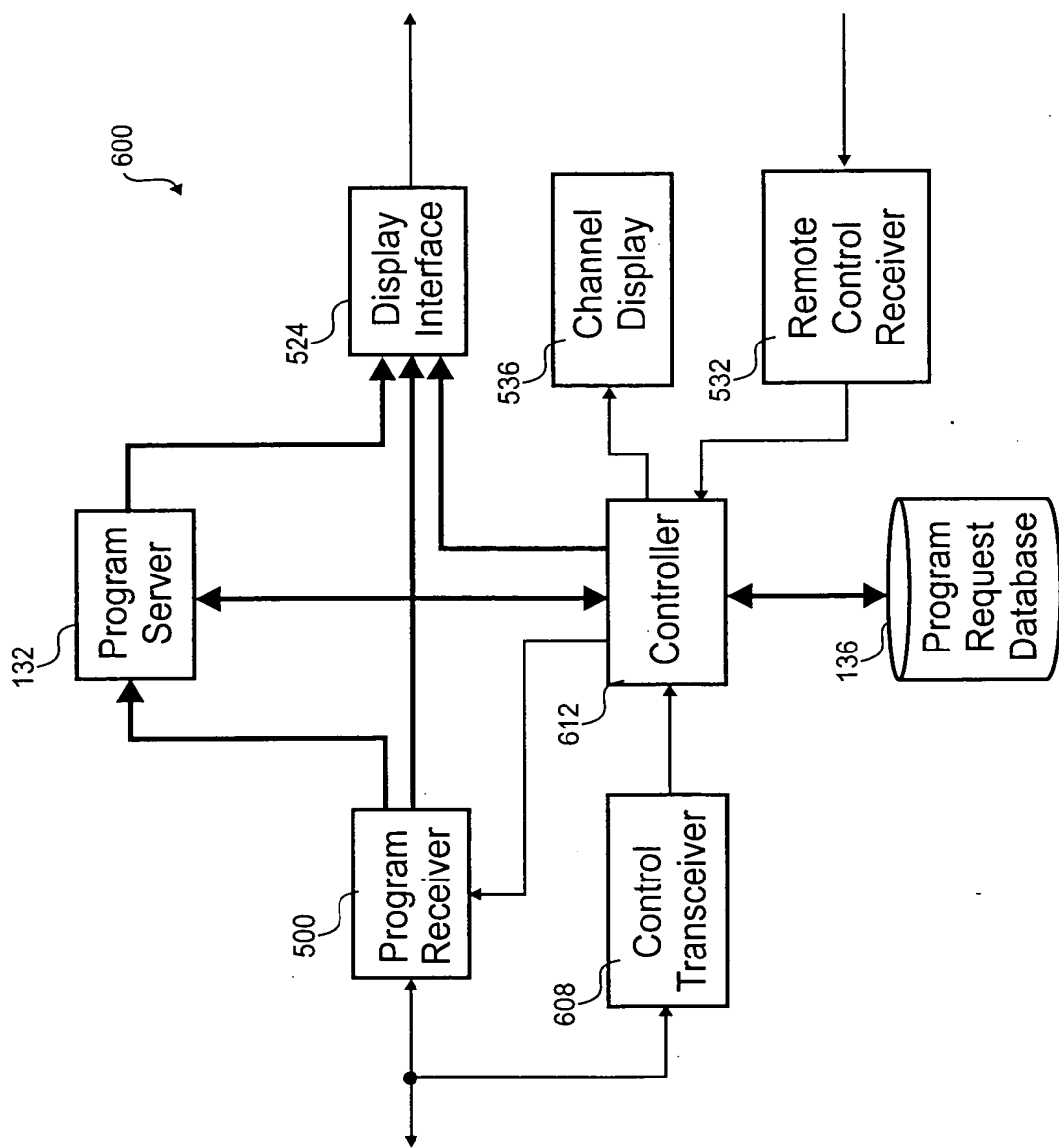


Fig. 6

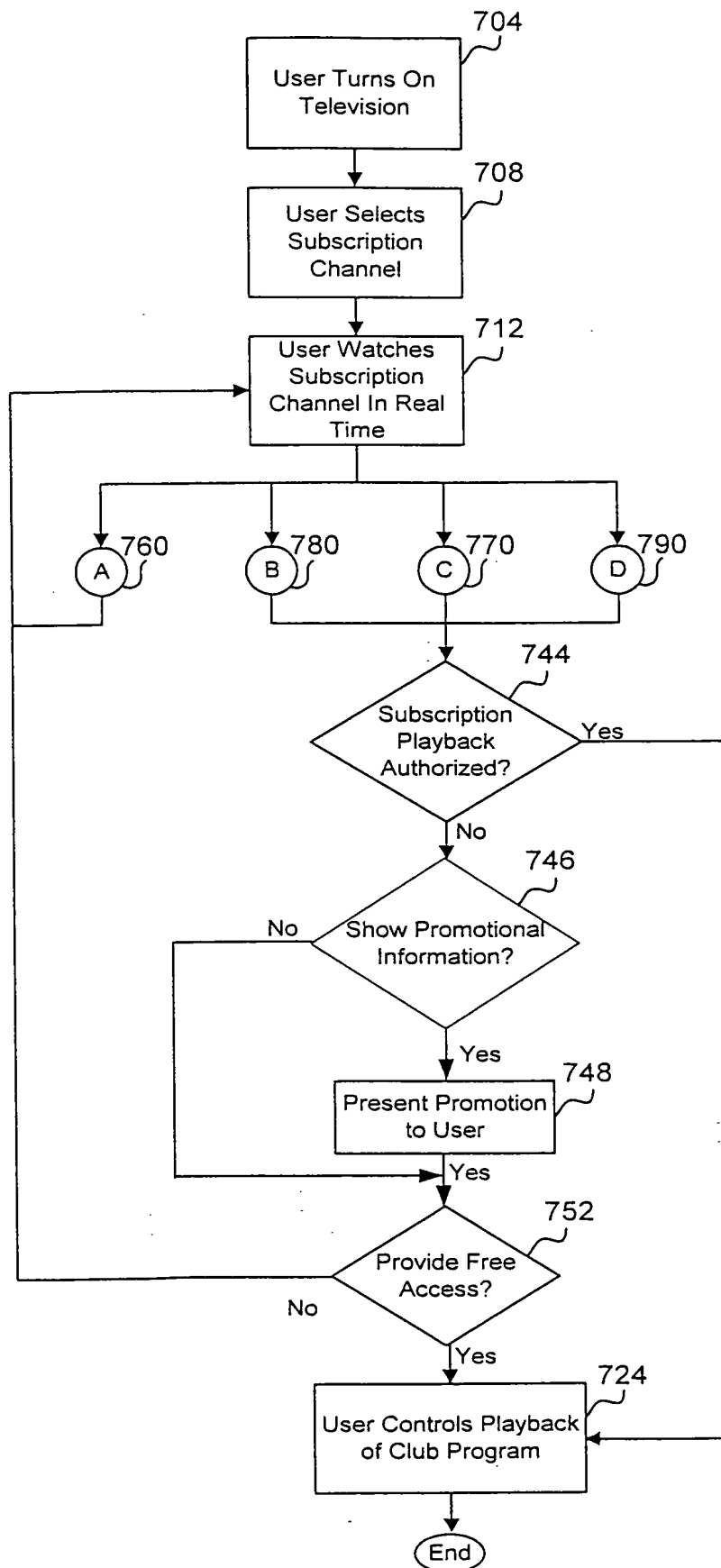


FIG. 7

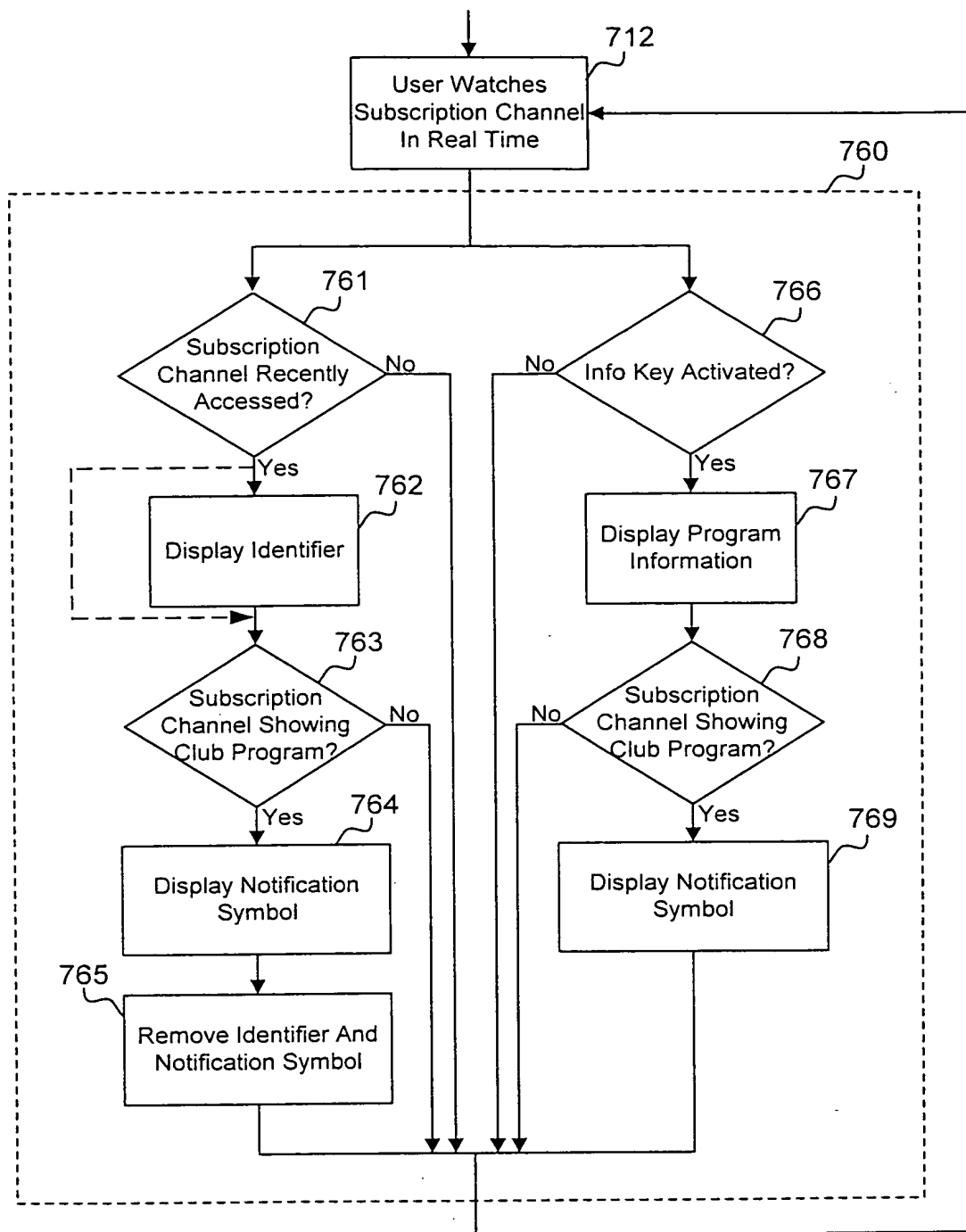


FIG. 7A

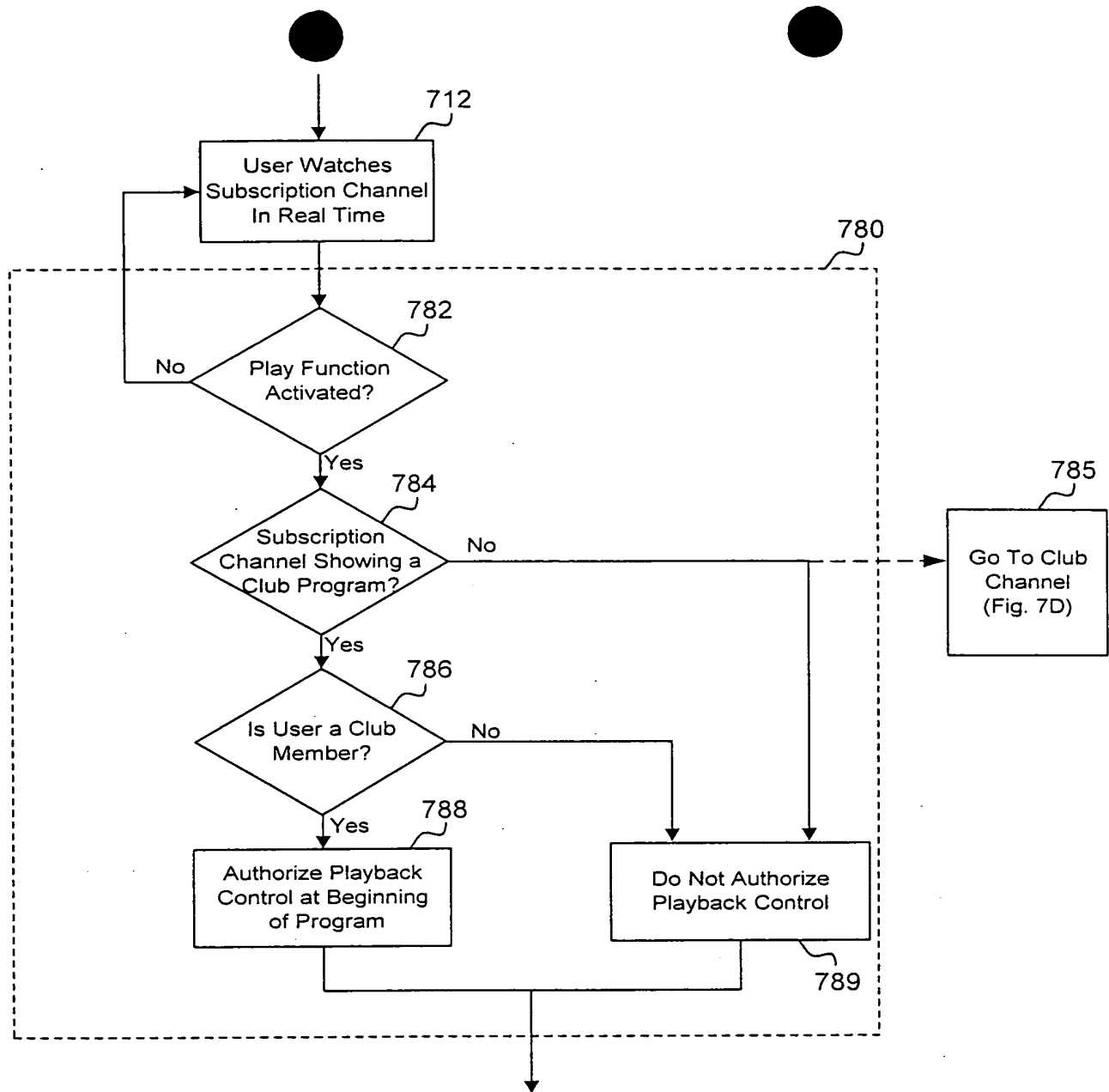


FIG. 7B

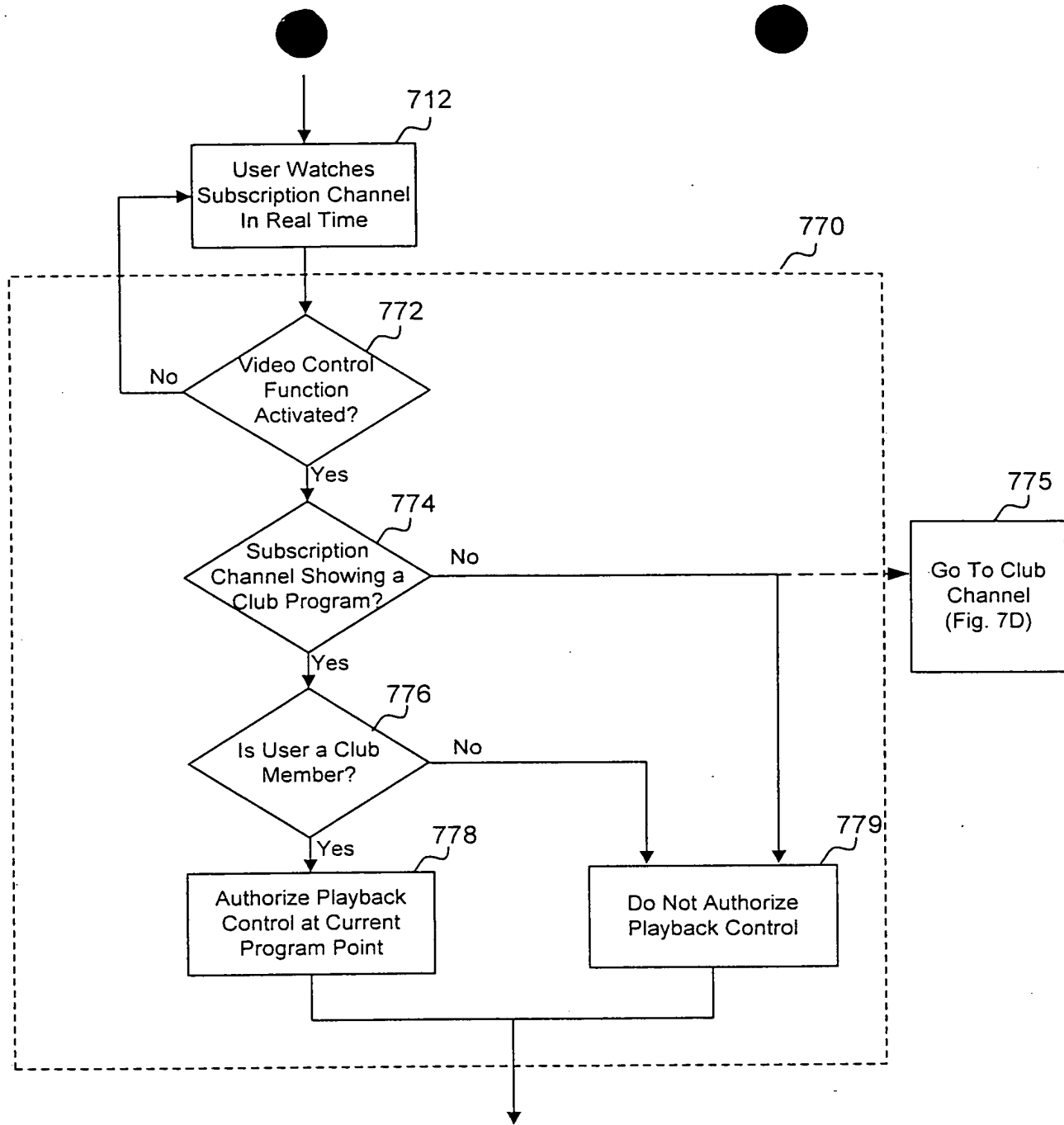


FIG. 7C

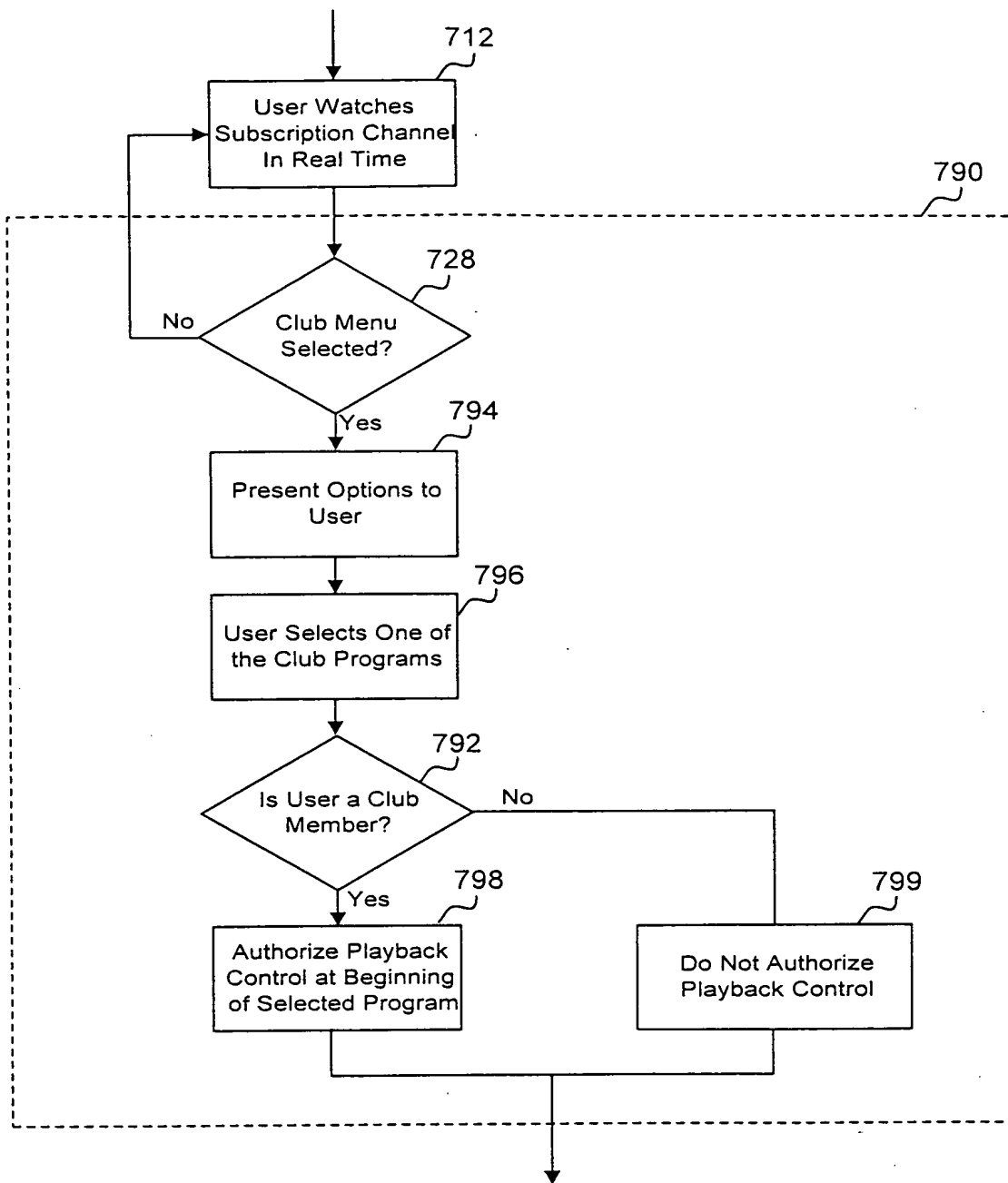


FIG. 7D

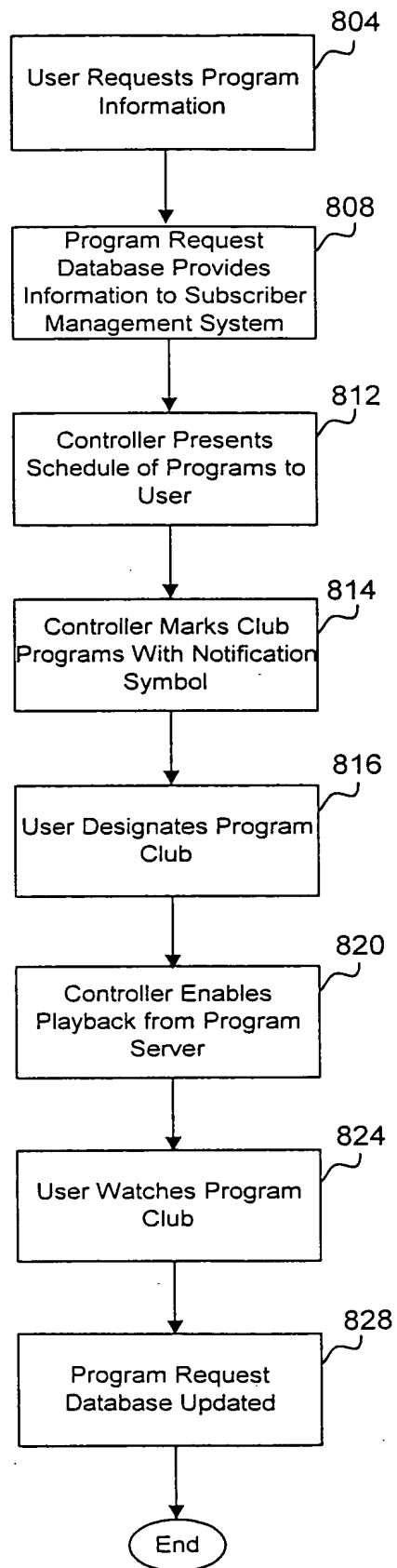


FIG. 8A

	6:00	6:30	7:00	7:30	8:00	8:30	9:00	9:30	10:00	10:30	11:00
Ch. A	840-1		840-2	☆	842	840-3	☆	840-1	840-4	☆	842
Ch. B		840-5		842	840-4		842	840-6	☆		840-1
Ch. C		840-7	☆		840-7	☆	840-8	840-9			
Ch. D	840-8		840-10					840-10		☆	842
Ch. E		840-11	842		840-4	842	840-3	840-8			
Ch. F		840-3	☆	840-6	☆		840-10				842
Ch. G		840-12		840-10			840-7			☆	

FIG. 8B

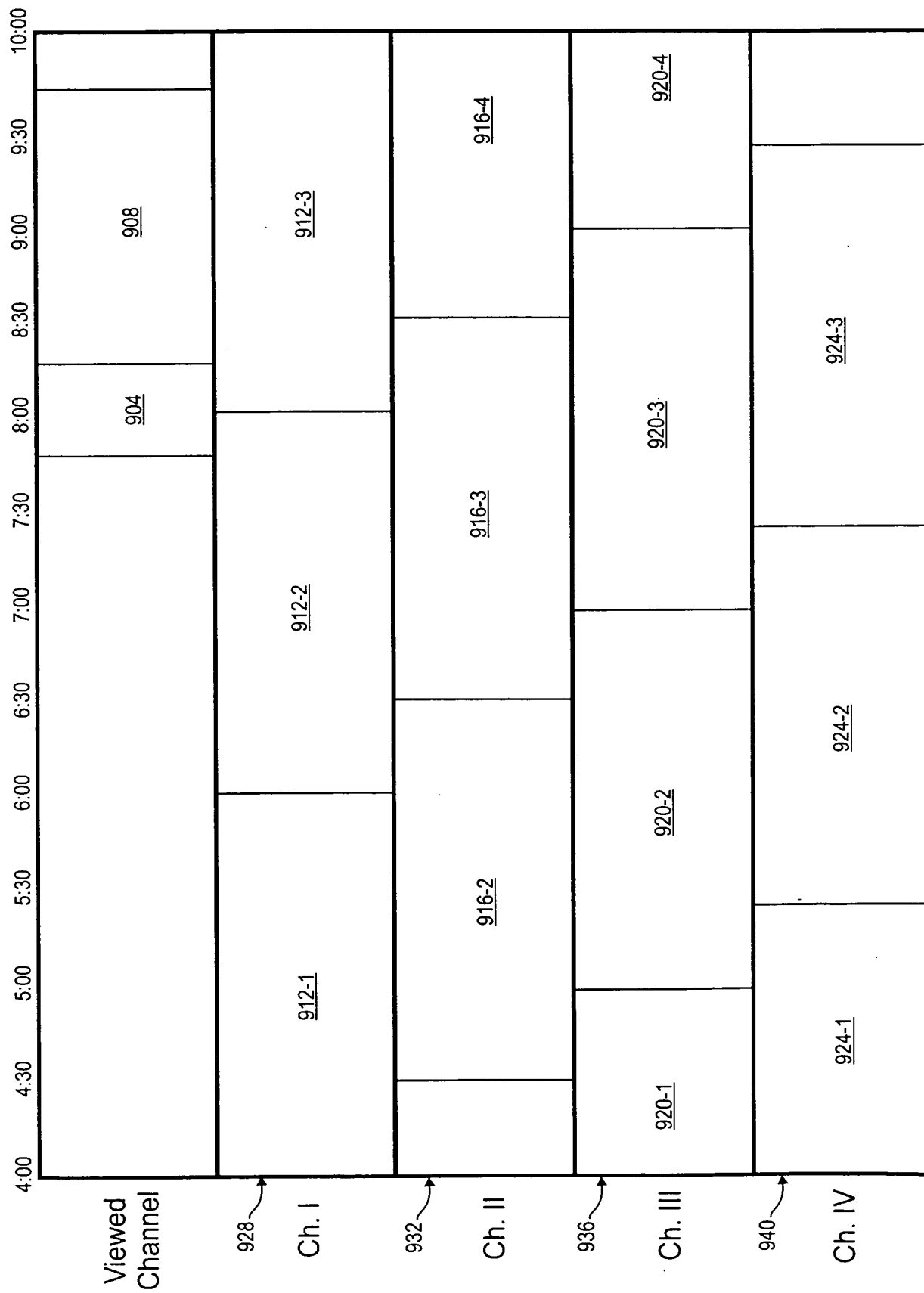


Fig. 9A

FIG. 9B is a diagram of a time slot grid for a television channel. The grid is divided into four channels: Viewed Channel, Ch. I, Ch. II, and Ch. IV. The time slots are labeled with numbers 960, 964, 968, and 972. The time slots are arranged in a grid with 10 columns and 4 rows. The columns are labeled with times from 4:00 to 10:00 in 30-minute increments. The rows are labeled with channel names: Viewed Channel, Ch. I, Ch. II, and Ch. IV. The Viewed Channel row is divided into four segments: 4:00-8:00 (labeled 960), 8:00-8:30 (labeled 964), 8:30-9:00 (labeled 968), and 9:00-10:00 (labeled 972). The Ch. I, Ch. II, and Ch. IV rows are each divided into four segments: 4:00-5:00 (labeled 960), 5:00-6:00 (labeled 964), 6:00-7:00 (labeled 968), and 7:00-8:00 (labeled 972). The Ch. II row is also divided into four segments: 8:00-8:30 (labeled 964), 8:30-9:00 (labeled 968), 9:00-9:30 (labeled 964), and 9:30-10:00 (labeled 968). The Ch. IV row is also divided into four segments: 8:00-8:30 (labeled 964), 8:30-9:00 (labeled 968), 9:00-9:30 (labeled 964), and 9:30-10:00 (labeled 968). The grid is labeled 958 in the top right corner.

	4:00	4:30	5:00	5:30	6:00	6:30	7:00	7:30	8:00	8:30	9:00	9:30	10:00
942 Viewed Channel									960	964	968	972	
944 Ch. I	960	960	960	960	960	960	960	960	960	960	960	960	960
948 Ch. II	964	964	964	964	964	964	964	964	964	964	964	964	964
952 Ch. III	968	968	968	968	968	968	968	968	968	968	968	968	968
956 Ch. IV	972	972	972	972	972	972	972	972	972	972	972	972	972

Fig. 9B

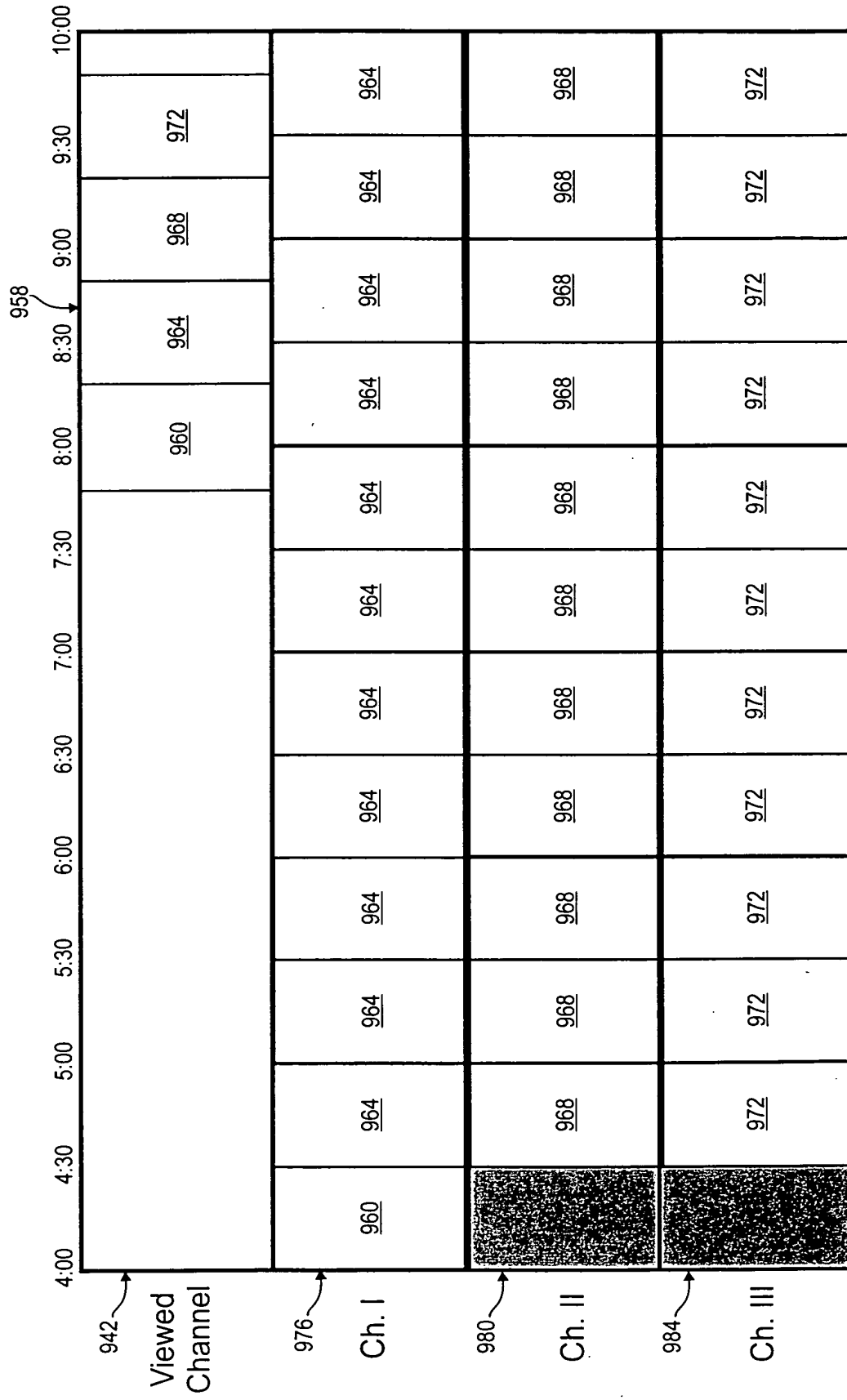


Fig. 9C

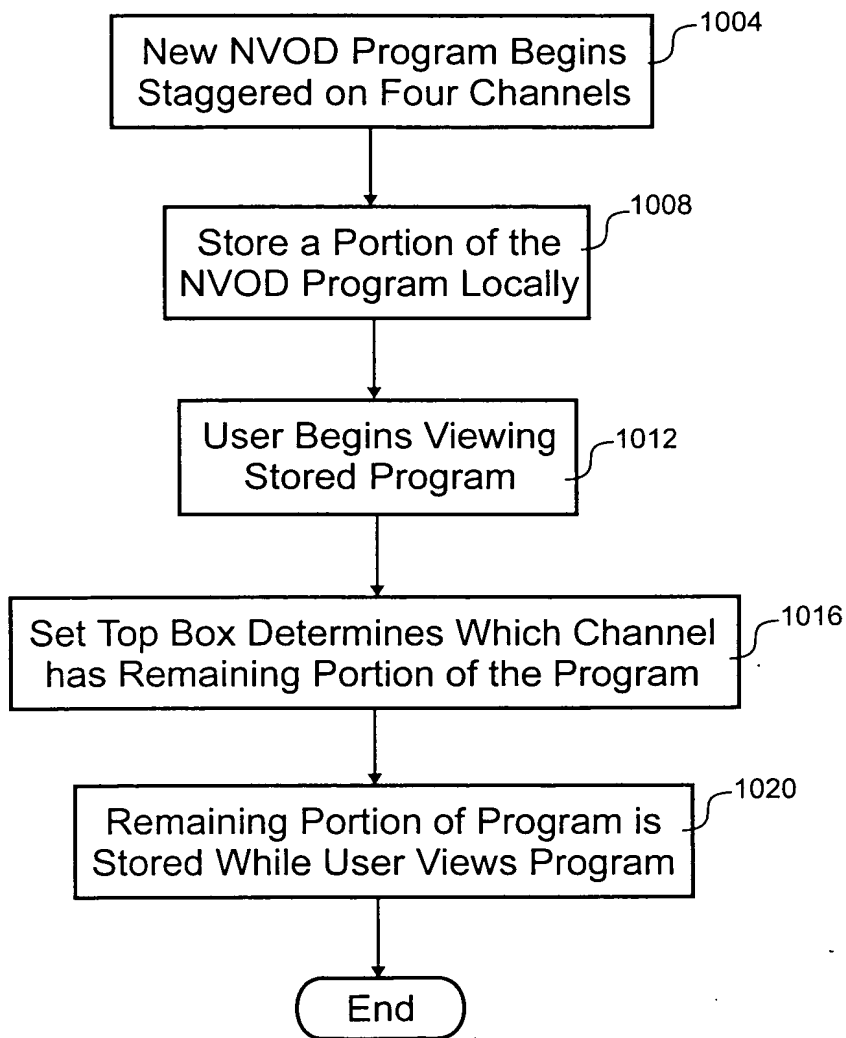


Fig. 10A

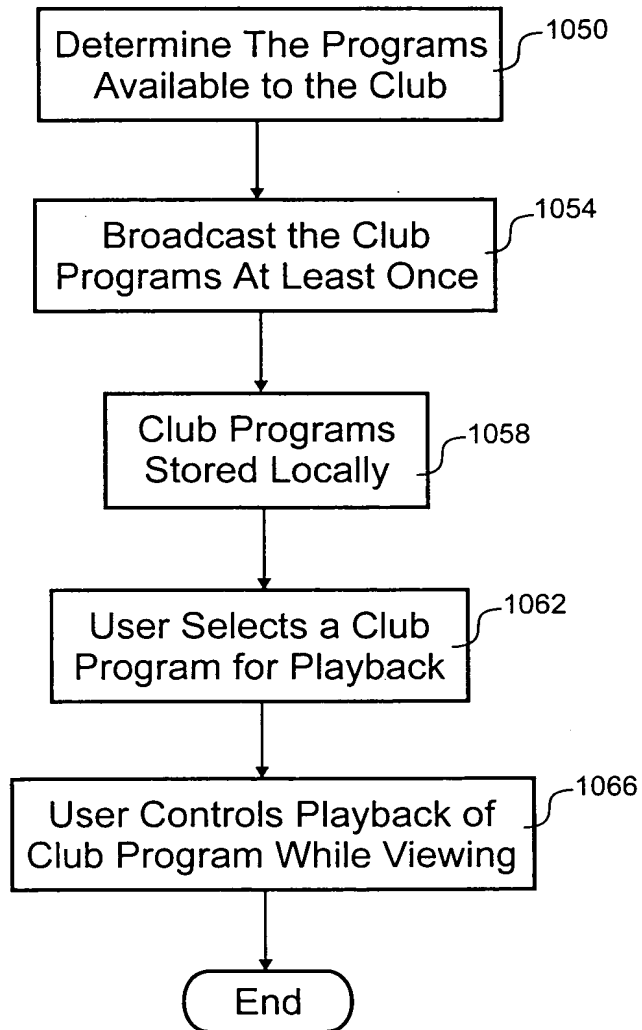


Fig. 10B

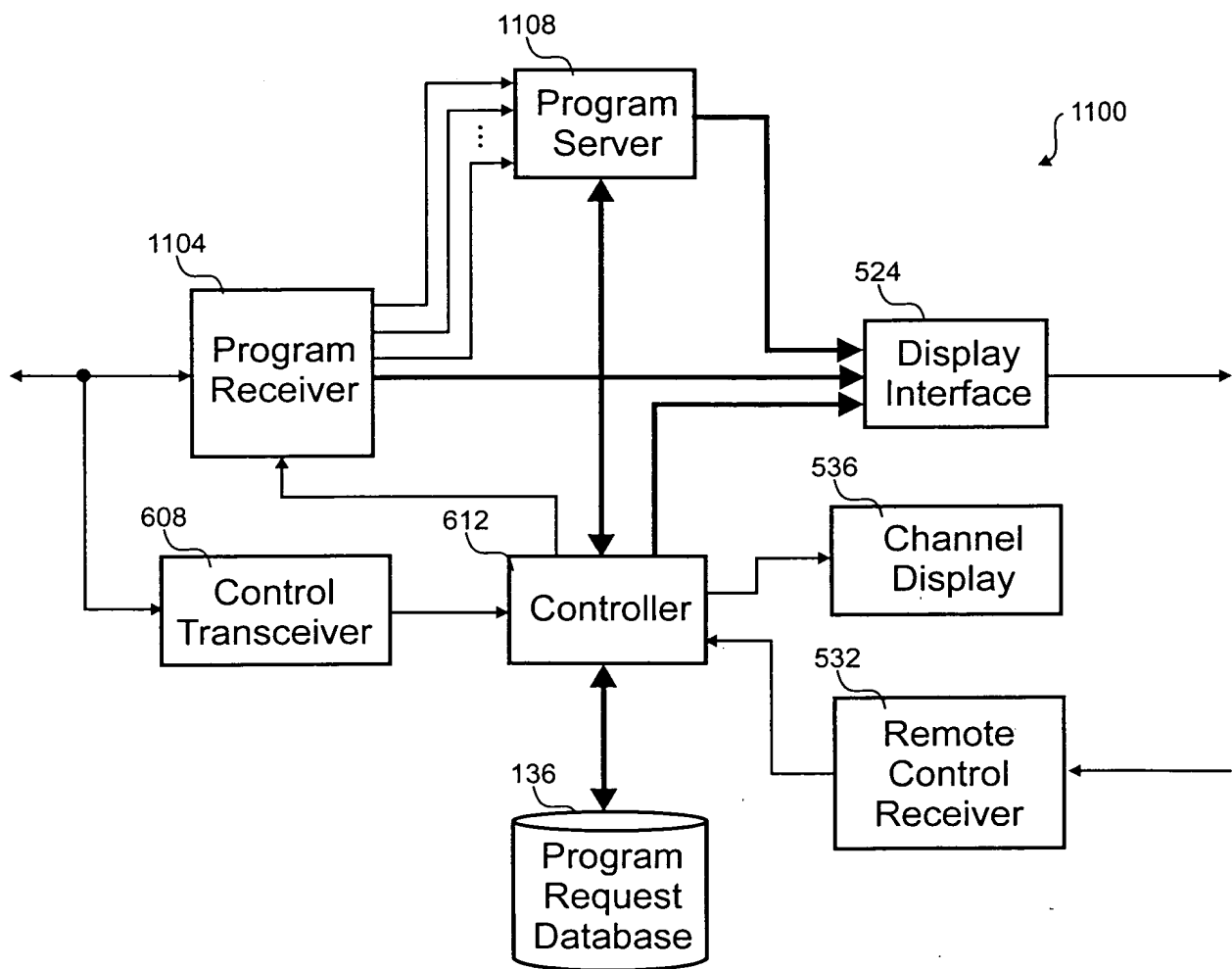


Fig. 11

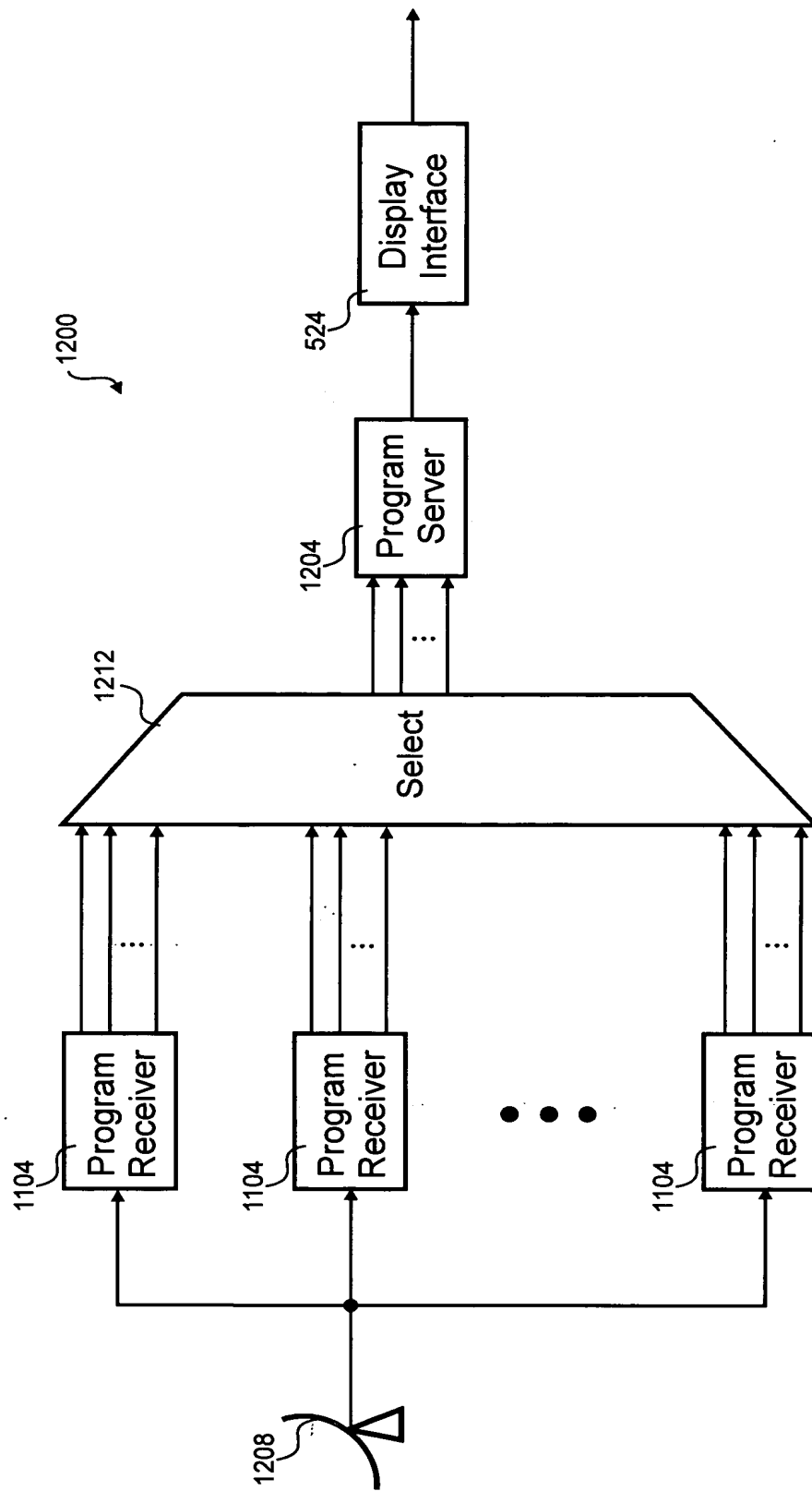


Fig. 12A

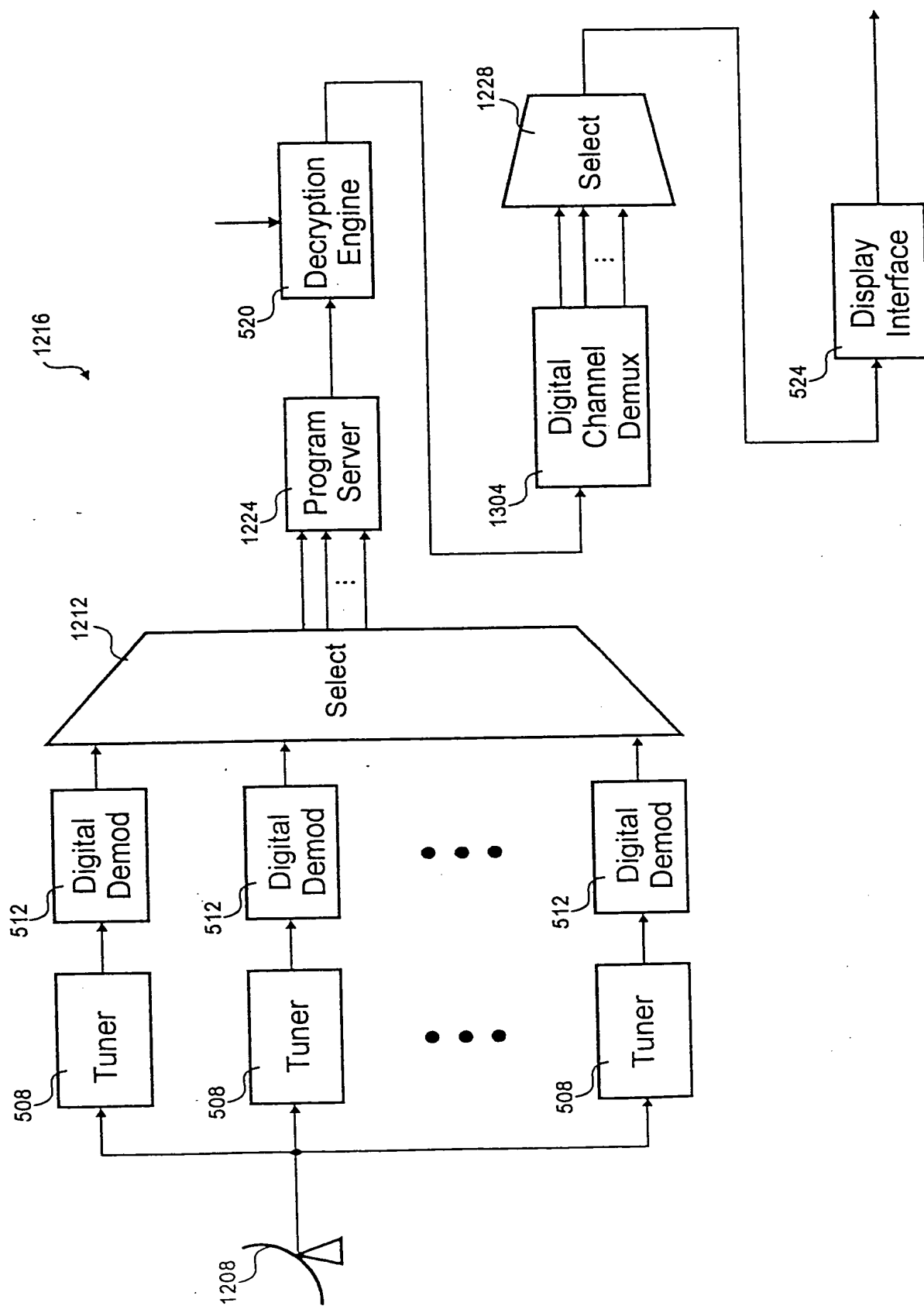


Fig. 12B

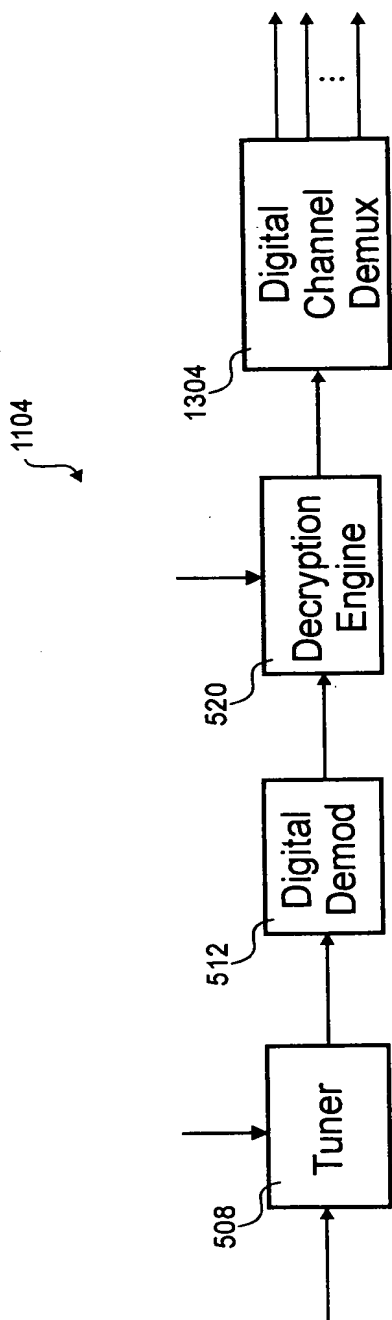
[illegible]

Fig. 13A

FIG. 13B

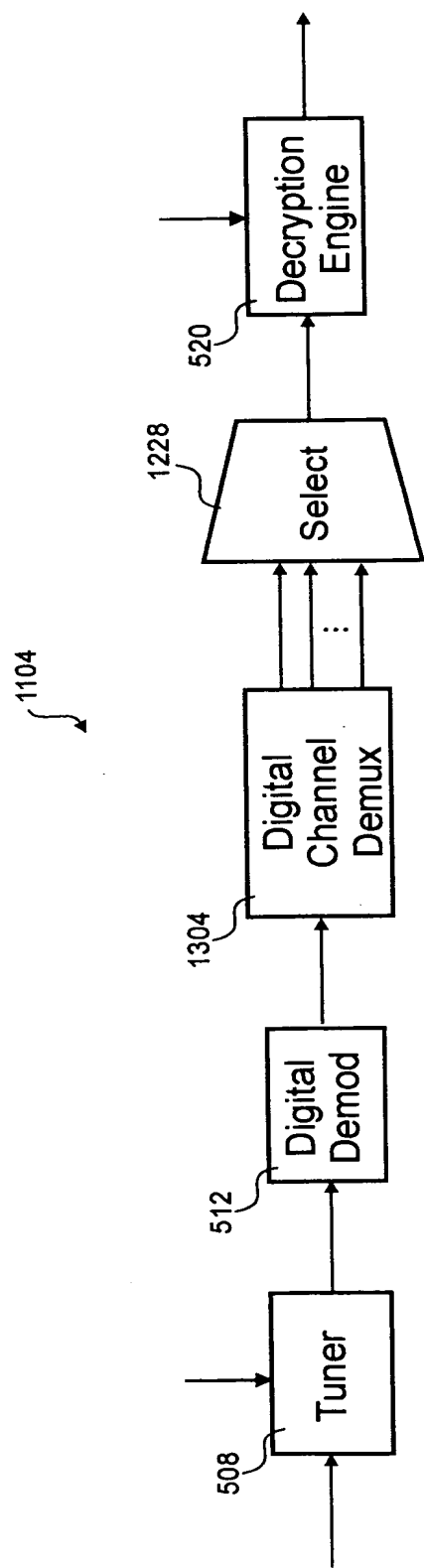


Fig. 13B

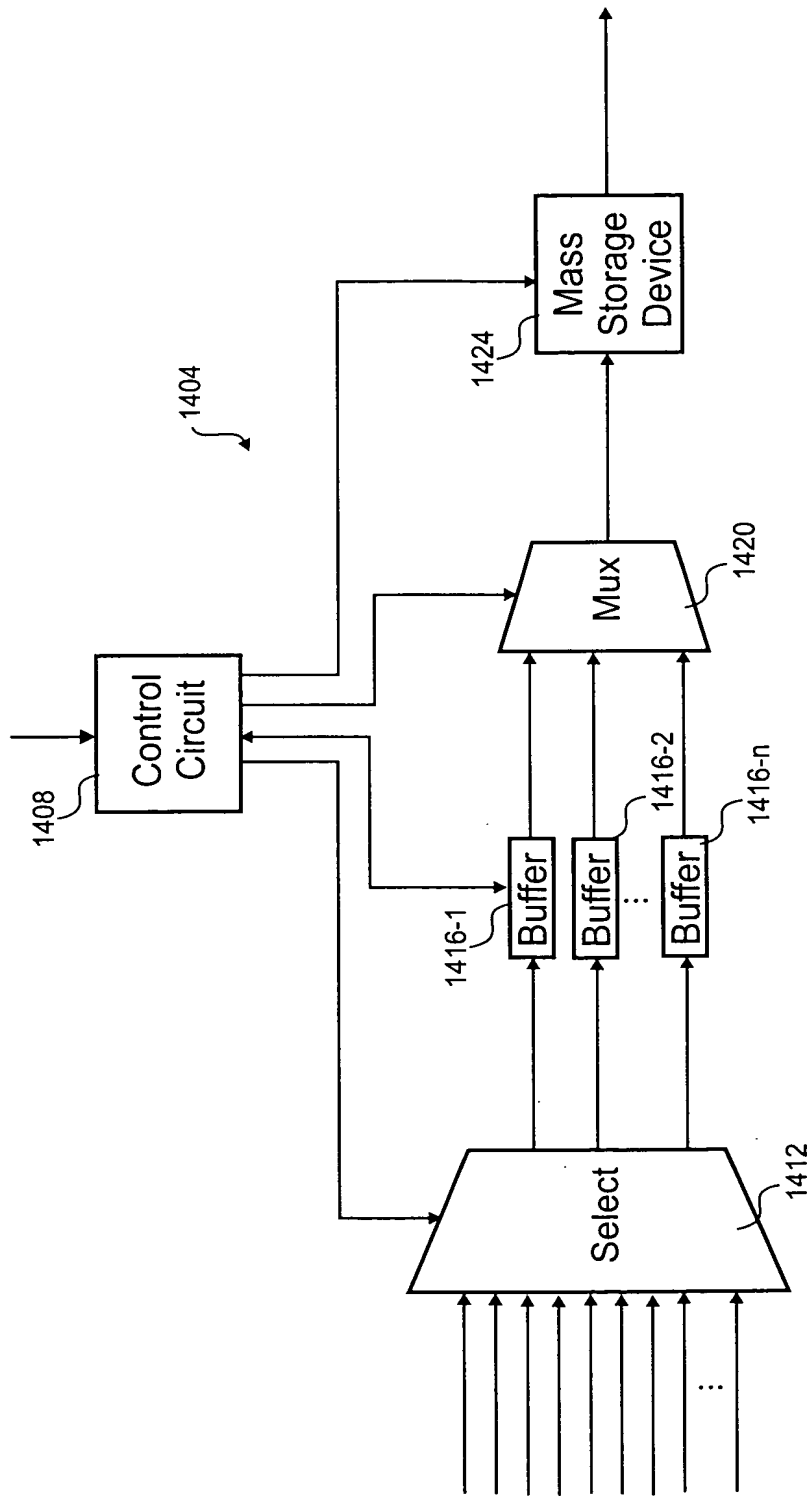


Fig. 14

FIG. 15 is a block diagram of a system 1504, according to one embodiment. The system 1504 includes a control circuit 1508, a select device 1512, a multiplexer (Mux) 1516, a mass storage device 1520, and another select device 1524. The control circuit 1508 is connected to the select device 1512, the Mux 1516, the mass storage device 1520, and the select device 1524. The select device 1512 receives multiple inputs (indicated by arrows) and outputs a signal to the Mux 1516. The Mux 1516 receives multiple inputs (indicated by arrows) and outputs a signal to the mass storage device 1520. The mass storage device 1520 outputs a signal to the select device 1524, which then outputs a final signal.

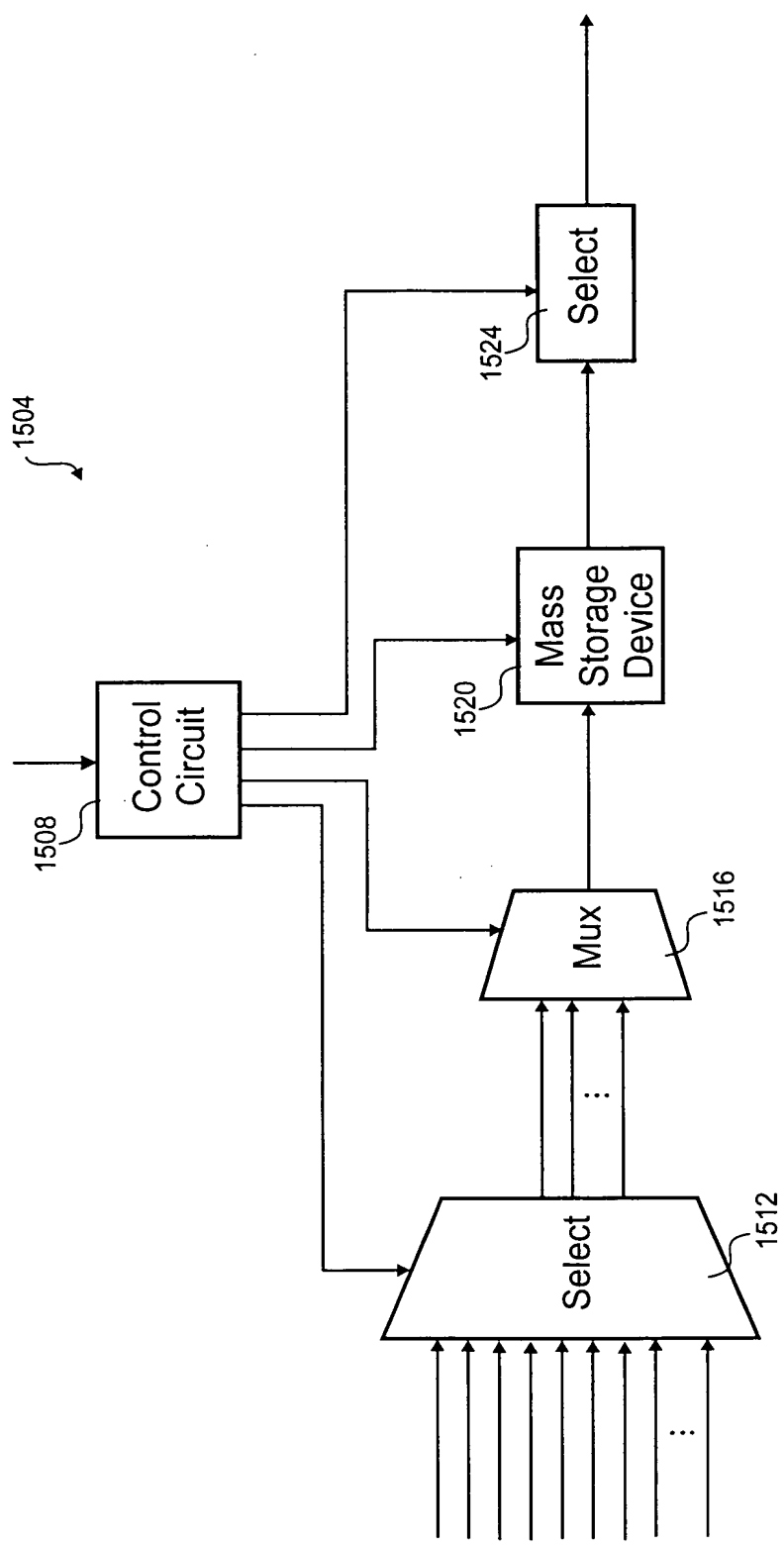


Fig. 15

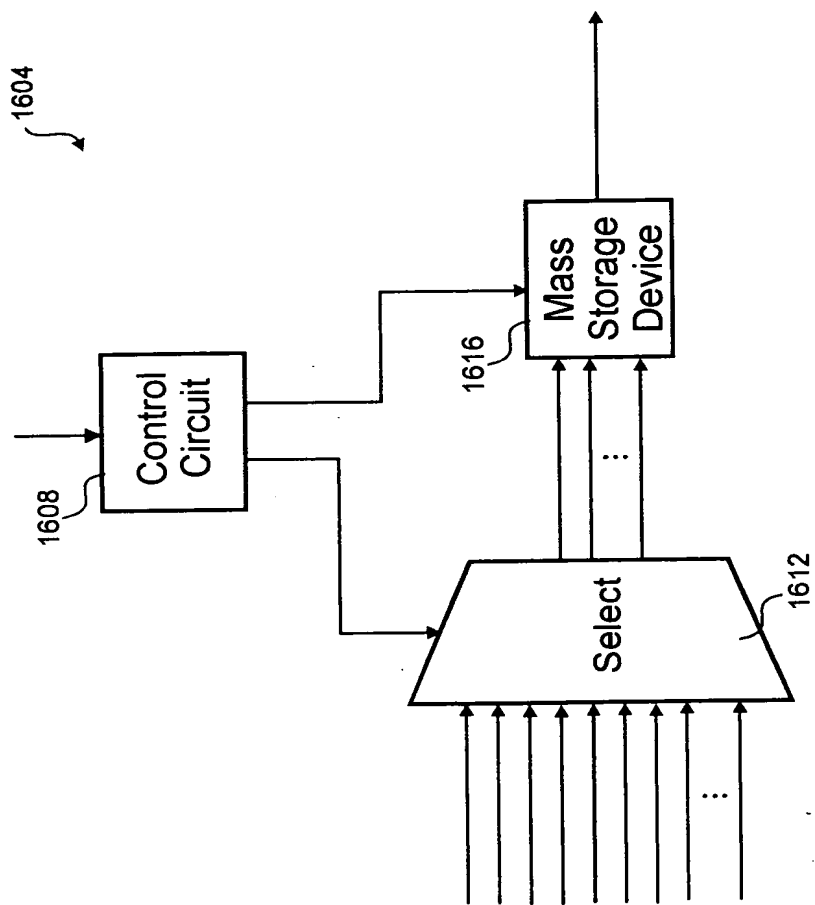


Fig. 16